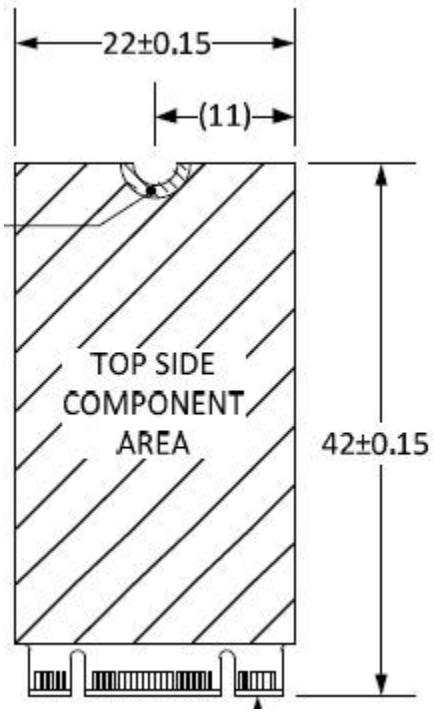
2016

RENICE X5A M.2 2242 SATAIII SSD DATA SHEET



Renice Technology Co., Limited

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1. Introduction

1.1 Product Overview

The Renice X5A M.2 series SSD is a high capacity SSD solution delivers extremely high performance up to 500MB/S read and 440MB/S write through the SATAIII 6.0Gbps interface. The X5A M.2 SSD is ideal for a variety of applications, including enterprise solutions where data throughput needs to be high, as well as industrial and military installations where the potential for high shock and vibration conditions exist.
X5A M.2 series SSD carries up to 512MB DDR3-1600 which gains high performance. With adopting SLC/ MLC NAND flash technology, and utilizing a unique firmware architecture, the X5A M.2 maximizes the bandwidth limitations of SATA III providing up to 75,000 input/output operations per second(IOPS).

1.2 Feature

● **Standard Serial ATA:** SATA III, 6.0Gbps (Backward compatible with SATA 1.5 and 3.0Gbps)
● **Form factor:** M.2 2242(NGFF) 42.0mm x 22.0mm x 3.5mm (L x W x H)
● **Connector:** 75pin SATA-based M.2 pinout
● **Performance:**
- Max Sequential Data Read/Write: 500MB/440MB/s
- 4Kb Random Read/Write IOPS: 70,000 / 75,000
- Access Time: <0.1ms
● **Capacities:** 32GB, 64GB, 128GB, 256GB (MLC)
16GB, 32GB, 64GB (SLC)
● **Power Management:**
- Input voltage: 3.3V (±5%)
- Support Hot Plug/Removal Function
● **Temperature ranges:**
– Operation: -40 to 85°C
– Storage: -50 to 95°C
● **Intelligent features:**
- Flash management algorithm: static and dynamic wear-leveling, bad block management algorithm
- Supports dynamic power management and SMART (Self-Monitoring, Analysis and Reporting Technology)
- Supports BCH ECC 66bits in 1KBytes
- Support Power Failure Protection
- Support over Voltage Protection
- Support AES 256bit Encryption (Optional)
- Support TRIM

- Support NCQ
- Support Devslp

● **MTBF:** >3,000,000 Hours @25C

2. Functional Block Diagram

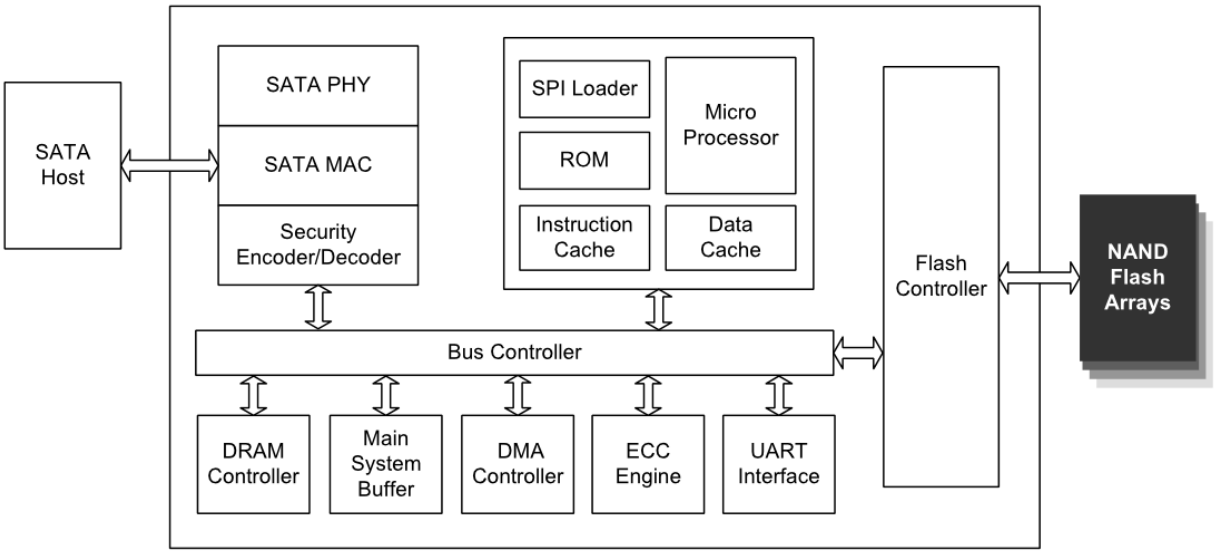


Figure 1: Renice X5A M.2 SATAIII SSD Block Diagram

3. Product Specifications

3.1 Physical Specifications

Table 1: Physical Specifications

Form Factor		M.2 Type2242
Dimensions	Length	42.0±0.25mm
	Width	22.0±0.25mm
	Height	3.5±0.25mm
Weight		<30g
Connector		75 pin

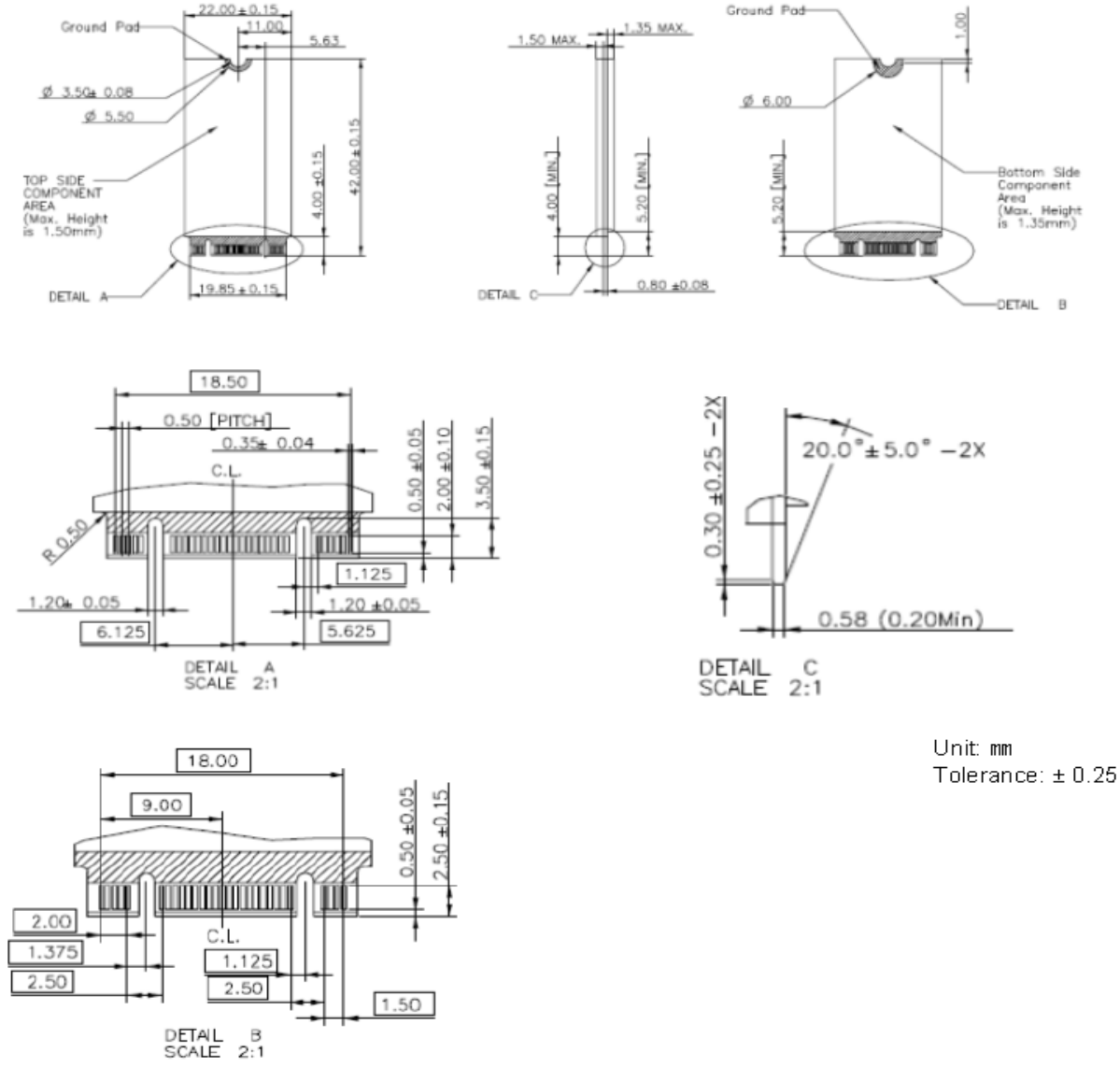


Figure 2: Renice X5A M.2 2242 SATAIII SSD mechanical dimensions

3.2 Host Interface

Industrial Standard SATA Revision 3.1 compliant
Industrial Standard ATA/ATAPI-8 ACS-2 command compliant
Supports SATA interface rate of 6Gb/s(backward compatible to 1.5Gb/s and 3Gb/s)
Native Command Queuing (NCQ): up to 32 commands
S.M.A.R.T. command transport (SCT) technology
SATA Device Sleep (DevSlp)
Data Set Management command (TRIM)
Supports 28bit and 48bit LBA mode commands

3.3 Capacity

Table 2: Capacity Specification

Parameter.	LBA Counts(512Byte)	Over-provision (%)
16GB		6.25
32GB	61,865,984	6.25
64GB	123,731,968	6.25
128GB	247,463,936	6.25
256GB	494,927,872	6.25

Table 3: Performance

MLC	**Capacity**	**32GB**	**64GB**	**128GB**	**256GB**
	Sequential Read(max)	300MB/s	500MB/s	500MB/s	500MB/s
	Sequential Write(max)	45MB/s	95MB/s	190MB/s	300MB/s
	4KB Random Read(QD32)	220MB/S	230MB/S	250MB/S	260MB/S
	4KB Random Write(QD32)	40MB/S	80MB/S	150MB/S	240MB/S
SLC	**Capacity**	**16GB**	**32GB**	**64GB**	
	Sequential Read(max)	350MB/S	500MB/S	500MB/S	
	Sequential Write(max)	120MB/S	260MB/S	440MB/S	
	4KB Random Read(QD32)	260MB/S	280MB/S	300MB/S	
	4KB Random Write(QD32)	100MB/S	250MB/S	300MB/S	

Note: Performance is based on CrysalDiskMark3.03 with file size 1000MB

4. Interface Description

4.1 Pin Assignment

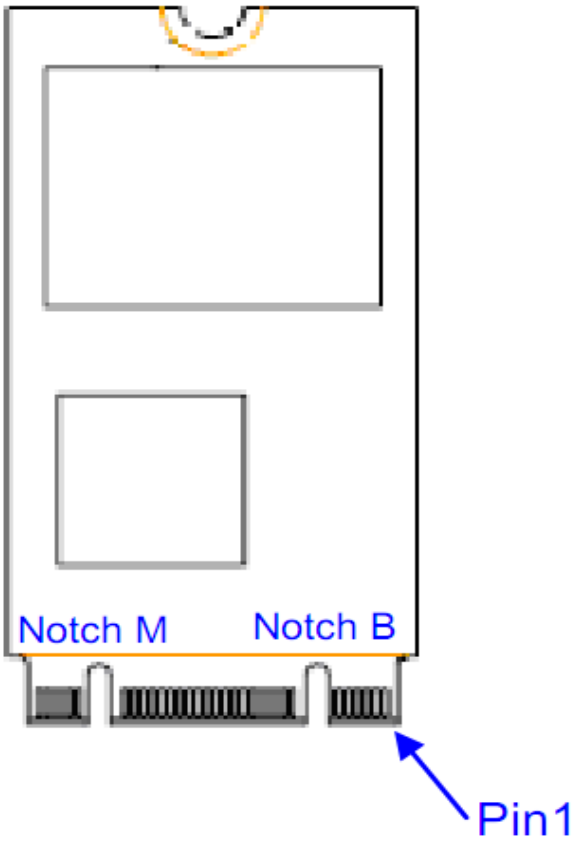


Figure 3: Pin Assignments

4.2 Pin Description

Table 3: Pin Assignments

Pin	Type	Description
1	CONFIG_3	Ground (according to M.2 configurations for SSD-SATA definition)
2	3.3V	Supply Pin, 3.3V
3	GND	Ground
4	3.3V	Supply pin, 3.3V
5	No connect	No connect
6	Not available	No connect (used for other purposes)
7	Not available	No connect (used for other purposes)
8	Not available	No connect (used for other purposes)
9	No connect	No connect
10	DAS/DSS	Device Activity Signal/Disable Staggered Spin-up
11	No connect	No connect (used for other purposes)
12	(removed for key)	Mechanical notch B
13	(removed for key)	Mechanical notch B
14	(removed for key)	Mechanical notch B
15	(removed for key)	Mechanical notch B
16	(removed for key)	Mechanical notch B
17	(removed for key)	Mechanical notch B
18	(removed for key)	Mechanical notch B
19	(removed for key)	Mechanical notch B
20	Not available	No connect (used for other purposes)
21	CONFIG_0	Ground (according to M.2 configurations for SSD-SATA definition)
22	Not available	No connect (used for other purposes)
23	Not available	No connect (used for other purposes)
24	Not available	No connect (used for other purposes)

25	Not available	No connect (used for other purposes)
26	Not available	No connect (used for other purposes)
27	GND	Ground
28	Not available	No connect (used for other purposes)
29	PERn1	Not used
30	Not available	No connect (used for other purposes)
31	PERp1	Not used
32	Not available	No connect (used for other purposes)
33	GND	Ground
34	Not available	No connect (used for other purposes)
35	PETn1	Not used
36	Not available	No connect (used for other purposes)
37	PETp1	Not used
38	DEVSLP	Device Sleep, input. If driven high the host is informing the SSD to enter a low power state
39	GND	Ground
40	Not available	No connect (used for other purposes)
41	SATA-Tx+	Host receiver differential signal pair
42	Not available	No connect (used for other purposes)
43	SATA-Tx-	Host receiver differential signal pair
44	Not available	No connect (used for other purposes)
45	GND	Ground
46	Not available	No connect (used for other purposes)
47	SATA-Rx-	Host transmitter differential pair
48	Not available	No connect (used for other purposes)
49	SATA-Rx+	Host transmitter differential pair
50	PERST#	Not used
51	GND	Ground

52	CLKREQ#	Not used
53	REFCLKN	Not used
54	PEWAKE#	Not used
55	REFCLKP	Not used
56	MFG1	Manufacturing pin. Use determined by vendor (no connect on a host)
57	GND	Ground
58	MFG2	Manufacturing pin. Use determined by vendor (no connect on a host)
59	(removed for key)	Mechanical notch M
60	(removed for key)	Mechanical notch M
61	(removed for key)	Mechanical notch M
62	(removed for key)	Mechanical notch M
63	(removed for key)	Mechanical notch M
64	(removed for key)	Mechanical notch M
65	(removed for key)	Mechanical notch M
66	(removed for key)	Mechanical notch M
67	Not available	No connect (used for other purposes)
68	SUSCLK	Not used
69	CONFIG_1	Ground
70	3.3V	Supply pin, 3.3V
71	GND	Ground
72	3.3V	Supply pin, 3.3V
73	GND	Ground
74	3.3V	Supply pin, 3.3V
75	CONFIG_2	Ground

5. Power Specifications

5.1 Operating Voltage

Operating voltage: 3.3V (±5%)

5.2 Power Supply Voltage

1.2V for Core, 1.5V for DDR, 3.3V for NAND and 1.8V for NAND IO

5.3 Power Consumption (typical)

Operation (Read/Write) –1.2W/4.5W
Idle - 0.6W
Standby - 0.45W

6. Reliability Specification

6.1 Environment

Table 4: Environmental Specifications

Item	Features	
Temperature	Operation	Industrial: -40~+85°C
Humidity	5-95%	
Vibration	10Hz-2000Hz, 16.4 G (X, Y, Z axis, 1 hour /axis)	
Shock	Peak Acceleration: 1,500 G, 0.5ms(Half-sine wave, ±X,±Y,±Z axis, 1 time/axis) Peak Acceleration: 50 G, 11ms(Half-sine wave, ±X,±Y,±Z axis, 3 times/axis)	

6.2 Wear-leveling

Renice X5A M.2 SSD support both static and dynamic wear-leveling, these two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

6.3 H/W ECC and EDC for NAND Flash

BCH ECC 66 bits in 1024 bytes.

6.4Power Failure Protection

Renice X5A M.2 SATA SSD adopts on board SDRAM and Capacitors. Data will be written to SDRAM firstly and then to NAND flash. In case of Power Loss, the detection circuit will tell the controller, and then the controller will refresh SDRAM data to NAND Flash at first and write protect NAND flash.

6.5 Over voltage and inrush current protection

The over voltage and inrush current protection mechanism of Renice X5A M.2 SATAIII is designed to be a protect circuitry on Device Power In. Once the current or voltage is exceeded, it will be pull down to the normal value in very short time to protect the drive.

6.6 Endurance

Write endurance: >12 years @ 100GB write/ day (256GB MLC)
Read endurance: unlimited

6.7 MTBF

MTBF (Mean Time between Failures) of Renice X5A M.2 SSD: >3,000,000 Hours @25C

7. Supported ATA Command Lists

Table 5: Support ATA Command Lists

Command	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute device diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Initialize Drive Parameters	91h	Non-data
Read DMA	C8h	DMA
Read Log Ext	2Fh	PIO data-in
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Power Management Feature Set		
Check Power Mode	E5h or 98h	Non-data
Idle	E3h or 97h	Non-data
Idle Immediate	E1h or 95h	Non-data
Sleep	E6h or 99h	Non-data
Standby	E2h or 96h	Non-data
Standby Immediate	E0h or 94h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out

SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute OFF-LINE Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-in
SMART Read Data	B0h	PIO data-in
SMART Read Threshold	B0h	PIO data-in
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

8. SMART Feature Set

The Renice X5A supports the SMART command set and defines some vendor-specific data to report spare/bad block numbers in each memory management unit.

Table 6: SMART Feature Register Values

Command Name	Command Code
SMART READ DATA	D0h
SMART Read Attribute Threshold	D1h
SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h
SMART SAVE ATTRIBUTE VALUES	D3h
SMART EXECUTE OFF-LINE IMMIDIATE	D4h
SMART READ LOG	D5h
SMART WRITE LOG	D6h
SMART ENABLE OPERATIONS	D8h
SMART DISABLE OPERATIONS	D9h
SMART RETURN STATUS	DAh

8.1 SMART Data Structure

The following 512bytes make up the device SMART data structure. Users can obtain the data using the “Read Data” command (D0h).

Table 7: SMART Data Structure

Byte	F / V	Description
0 - 1	X	Revision code
2 - 361	X	Vendor specific (see 4.3.2)
362	V	Off-line data collection status
363	X	Self-test execution status byte
364 - 365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368 - 369	F	SMART capability
370	F	Error logging capability • 7-1 Reserved • 0 1 = Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375 - 385	R	Reserved
386 - 395	F	Firmware version/date code
396 - 399	F	Reserved
400 - 405	F	‘SM2246’
406 - 510	X	Vendor specific
511	V	Data structure checksum

Notes:

1. F = content (byte) is fixed and does not change.
2. V = content (byte) is variable and may change depending on the state of the device or the commands executed by the device.
3. X = content (byte) is vendor specific and may be fixed or variable.
4. R = content (byte) is reserved and shall be zero.

8.2 SMART Attributes

The following table defines the vendor specific data in byte 2 to 361 of the 512byte SMART data.

Table 8: SMART Data Vendor-specific Attributes

Attribute ID (hex)	Raw Attribute Value							Attribute Name
01	MSB	00	00	00	00	00	00	Read error rate
05	LSB	MSB	00	00	00	00	00	Reallocated sectors count
09	LSB			MSB	00	00	00	Power-on hours
0C	LSB			MSB	00	00	00	Power cycle count
A0	LSB			MSB	00	00	00	Uncorrectable sector count when read/write
A1	LSB	MSB	00	00	00	00	00	Number of valid spare block
A3	LSB	MSB	00	00	00	00	00	Number of initial invalid block
A4	LSB			MSB	00	00	00	Total erase count
A5	LSB			MSB	00	00	00	Maximum erase count
A6	LSB			MSB	00	00	00	Minimum erase count
A7	LSB			MSB	00	00	00	Average erase count
A8	LSB			MSB	00	00	00	Max erase count of spec
A9	LSB			MSB	00	00	00	Remain Life (percentage)
AF	LSB			MSB	00	00	00	Program fail count in worst die
B0	LSB	MSB	00	00	00	00	00	Erase fail count in worst die
B1	LSB			MSB	00	00	00	Total wearlevel count
B2	LSB	MSB	00	00	00	00	00	Runtime invalid block count
B5	LSB			MSB	00	00	00	Total program fail count
B6	LSB	MSB	00	00	00	00	00	Total erase fail count
BB	LSB			MSB	00	00	00	Uncorrectable error count
C0	LSB	MSB	00	00	00	00	00	Power-off retract count
C2	MSB	00	00	00	00	00	00	Controlled temperature
C3	LSB			MSB	00	00	00	Hardware ECC recovered
C4	LSB			MSB	00	00	00	Reallocation event count
C6	LSB			MSB	00	00	00	Uncorrectable error count off-line
C7	LSB	MSB	00	00	00	00	00	UltraDMA CRC error count
E1	LSB						MSB	Total LBAs written (each write unit = 32MB)
E8	LSB	MSB	00	00	00	00	00	Available reserved space
F1	LSB						MSB	Total LBAs written (each write unit = 32MB)
F2	LSB						MSB	Total LBAs read (each read unit = 32MB)

9. Ordering Information

Table 9: Valid Combinations

Part Number	Description
RIM032-SX5AN-42	X5A M.2 2242 SATAIII 32GB MLC Industrial SSD
RIM064-SX5AN-42	X5A M.2 2242 SATAIII 64GB MLC Industrial SSD
RIM128-SX5AN-42	X5A M.2 2242 SATAIII 128GB MLC Industrial SSD
RIM256-SX5AN-42	X5A M.2 2242 SATAIII 256GB MLC Industrial SSD
RIS016-SX5AN-42	X5A M.2 2242 SATAIII 16GB MLC Industrial SSD
RIS032-SX5AN-42	X5A M.2 2242 SATAIII 32GB MLC Industrial SSD
RIS064-SX5AN-42	X5A M.2 2242 SATAIII 64GB MLC Industrial SSD

10. Part Number Naming Rule

